Notice of Allowability	Application No.	Applicant(s)		
	09/905,392	MORRISH, ANDY	MORRISH, ANDY	
	Examiner	Art Unit		
	Paulos M. Natnael	2614		
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85 NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.31	S (OR REMAINS) CLOSED in (i) or other appropriate commur RIGHTS. This application is su	this application. If not inclu nication will be mailed in du	ded e course. THIS	
1. This communication is responsive to remarks filed April 1.	<u>4, 2005</u>			
2. The allowed claim(s) is/are <u>1-21</u> .				
3. The drawings filed on 13 July 2001 are accepted by the E	xaminer.			
 4. Acknowledgment is made of a claim for foreign priority of a) All b) Some* c) None of the: Certified copies of the priority documents have Certified copies of the priority documents have Copies of the certified copies of the priority documents have Copies of the certified copies of the priority documents have Copies of the certified copies of the priority documents have Certified copies of the certified copies of the priority documents have Tertified copies not received: Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONITHIS THREE-MONTH PERIOD IS NOT EXTENDABLE. 	re been received. The been received in Application occuments have been received. The communication to file a	Noin this national stage applic		
5. A SUBSTITUTE OATH OR DECLARATION must be subminformal PATENT APPLICATION (PTO-152) which give			NOTICE OF	
 6. CORRECTED DRAWINGS (as "replacement sheets") muter (a) including changes required by the Notice of Draftsper 1) hereto or 2) to Paper No./Mail Date (b) including changes required by the attached Examiner Paper No./Mail Date (b) hereto or 2) to Paper No./Mail Date (b) including changes required by the attached Examiner Paper No./Mail Date (b) hereto or 2) to Paper No./Mail Date (c) including changes required by the attached Examiner (b) hereto or 2) to Paper No./Mail Date (c) including changes required by the Notice of Draftsper (c) including changes required by the Notice of Draftsper (c) including changes required by the Notice of Draftsper (c) including changes required by the Notice of Draftsper (c) including changes required by the Notice of Draftsper (c) including changes required by the Attached Examiner (c) including changes required by the Notice of Draftsper (c) including changes required by the Attached Examiner (c) including changes (c)	rson's Patent Drawing Review 's Amendment / Comment or i 1.84(c)) should be written on the the header according to 37 CFR DSit of BIOLOGICAL MATE	n the Office action of drawings in the front (not to 1.121(d). RIAL must be submitted	•	
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☑ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/Paper No./Mail Date 4. ☑ Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. Interview Sur Paper No./M 08), 7. Examiner's A	Mail Date Amendment/Comment Statement of Reasons for A	liowance	

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DETAILED ACTION

Allowable Subject Matter

- 1. Claims **1-21** are allowed.
- 2. The following is an examiner's statement of reasons for allowance: the prior art fails to disclose the following combination in an apparatus for reducing noise effects associated with the vertical position of an on screen display image that uses a vertical flyback signal and a horizontal flyback signal in producing an image, comprising: a clock signal generator that is configured to produce multiple horizontal clock signals in response to the horizontal flyback signal, wherein each multiple horizontal clock signal has a different phase with respect to one another; a phase selection circuit that is configured to select one of the multiple horizontal clock signals such that an edge associated with the selected multiple horizontal clock signal is non-coincident with an edge associated with the vertical flyback signal; a blanking circuit that is configured [to] produce a blanking signal in response to the selected multiple horizontal clock signal such that the blanking signal determines the vertical position of the OSD image, whereby noise effects associated with at least one of the vertical flyback signal and the horizontal flyback signal are minimized, as in claim 1;

A method for minimizing jitter in the vertical position of an on screen display (OSD) image for a display device having a display screen, comprising: producing multiple horizontal clock signals that each have a different phase in response to a first horizontal! timing signal and a second horizontal timing signal, which the first horizon

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timing signal and the second horizontal timing signal are related; selecting one of the multiple horizontal clock signals as a new horizontal flyback signal such that the occurrence of an edge associated with the selected horizontal clock signal is non-coincident with an edge associated with a vertical flyback signal of the display device;

and producing a vertical blanking signal in response to the selected horizontal clock signal wherein the vertical blanking signal triggers the display device to count a predetermined number of blank horizontal lines from the top of the display screen prior to generating the OSD image such that the predetermined number of blank horizontal lines corresponds to the vertical position of the OSD image on the display screen, as in claim 13; and,

An apparatus for providing jitter reduction for an on screen display (OSD) window of a display device having a display screen, comprising: a means for generating horizontal timing signal that is configured to generate a first horizontal timing signal an second horizontal timing signal, the first horizontal timing singles and the second horizontal timing signal are related; a means for producing multiple horizontal clock signals that is configured to produce multiple horizontal clock signals in response to the horizontal timing signal and the second horizontal timing signal such that each of the multiple horizontal clock signals has a different phase; a means for selecting a multiple horizontal clock signal that is configured to select one of the multiple horizontal clock signals such that the occurrence of an edge corresponding to the selected horizontal dock signal is non-coincident with an edge associated with the vertical flyback signal; and a

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means for producing a vertical blanking signal that is configured to produce a vertical blanking signal in response to the selected horizontal clock signal wherein the vertical blanking signal triggers the display device to count a predetermined number of blank horizontal lines from the top of the display screen prior to generating the OSD image such that the predetermined number of blank horizontal lines corresponds to the vertical position of the OSD image on the display screen, whereby jitter in the vertical position of the OSD window is reduced, as in claim 19.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (571) 272-7354. The examiner can normally be reached on 10:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571)272-7353. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paulos M. Nathael Primary Examiner Art Unit 2614

July 6, 2005